What Is Claimed Is:

1. A method for programming a nonvolatile memory by a control system having a controller for controlling transfer of data to be programmed, the method comprising the steps of:

sequentially transferring and storing serial address bits from the exterior to the controller;

sequentially transferring and storing a first group of serial data bits from the exterior to the controller;

determining whether all the serial data bits of the first group are transferred to the controller;

transferring the first group of serial data bits to the nonvolatile memory when all the serial data bits of the first group are transferred to the controller; and

sequentially transferring and storing a second group of serial data bits to the controller, while programming the first group of serial data bits in the nonvolatile memory at the address indicated by the address bits.

2. The method of claim 1 further comprising, before the step of transferring the serial address bits to the controller, the steps of:

determining the capacity of the nonvolatile memory; and

setting an enable period of the programming in the nonvolatile memory according to the result of the step of determining the capacity of the nonvolatile memory.

3. The method of claim 1 further comprising, before the step of programming the first group of serial data bits in the nonvolatile memory, generating a voltage enable signal necessary for the programming.

4. The method of claim 1 wherein whether all the serial data bits are transferred to the controller is determined by detecting a stop bit in the serial data bits.

5. The method of claim 1, wherein the address is increased whenever all the serial data bits of the respective group, except the serial data bits of the first group, are transferred to the controller .

6. The method of claim 1, wherein each group of the serial data bit comprises 1 byte or more.

7. The method of claim 1, wherein the nonvolatile memory is embodied in the control system.

8. A control system comprising:

a memory chip having a nonvolatile memory for storing data bits and programming the stored data bits; and

a controller for determining the capacity of the nonvolatile memory, serially transferring a group of data bits to the nonvolatile memory based on the capacity of the nonvolatile

memory, and enabling the programming of the group of data bits in the nonvolatile memory while transferring a next group of data bits to the nonvolatile memory.

9. The control system of claim 8 wherein the memory chip further comprises a write buffer for receiving and storing the group of data bits from the controller, and transferring the stored group of data bits to the nonvolatile memory.

10. The control system of claim 9 wherein the memory chip further comprises an embodied voltage generator for generating a voltage necessary for the programming in the nonvolatile memory.

11. The control system of claim 8 wherein the controller comprises:

a data register for storing the group of data bits serially provided from exterior and transferring the group of data bits to the write buffer, the group of data bits being programmed in the nonvolatile memory;

an address register for storing address bits serially provided from exterior, and transferring the stored address bits to the nonvolatile memory, wherein the address bits are varied when the next group of data bits is transferred to the data register; and

a control logic for making the group of data bits and address bits in the data and address registers transferred to the write buffer and the nonvolatile memory respectively and enabling a program enable signal for the performing of the stored data bits in the nonvolatile memory.

12. The control system of claim 11 wherein the controller further comprises a byte select circuit for outputting a byte select signal indicating the capacity of the nonvolatile memory, wherein the control logic controls an enable period of the program enable signal based upon the byte select signal.

13. The control system of claim 12 wherein the transferring time of the group of serial data bits is the same or is longer than the enable period of the program enable signal.

14. The control system of claim 12 wherein the byte select circuit sets the byte select signal before the transferring of the address bits and the group of data bits are started.

15. The control system of claim 12 wherein the controller further comprises a command register for receiving information for the capacity of the nonvolatile memory.

16. The control system of claim 15 wherein the byte select circuit sets the byte select signal according to the information of the command register.

17. The control system of claim 12 wherein the byte select circuit sets the byte select signal by using one of a central processing unit of the control system and a ground voltage pin.